

Product Description

The SP4302 is a high linearity, 6-bit RF Digital Step Attenuator (DSA) covering a 31.5 dB attenuation range in 0.5 dB steps. This 50-ohm RF DSA provides both parallel and serial CMOS control interface operates on a single 3-volt supply and maintains high attenuation accuracy over frequency and temperature. It also has a unique control interface that allows the user to select an initial attenuation state at power-up. The SP4302 exhibits very low insertion loss and low power consumption. This functionality is delivered in a 4x4 mm QFN footprint.

The SP4302 is manufactured on SIPAT's UltraCMOS™ process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering the performance of GaAs with the economy and integration of conventional CMOS.

50 Ω RF Digital Attenuator
6-bit, 31.5 dB, DC – 4.0 GHz

Features

- Attenuation: 0.5 dB steps to 31.5 dB
- Flexible parallel and serial programming interfaces
- Unique power-up state selection
- Positive CMOS control logic
- High attenuation accuracy and linearity over temperature and frequency
- Very low power consumption
- Single-supply operation
- 50 Ω impedance
- Packaged in a 20 lead 4x4mm QFN

Figure 1. Functional Schematic Diagram

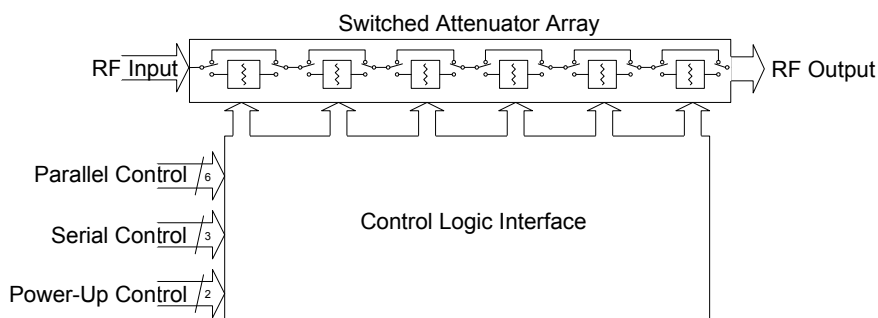


Figure 2. Package Type

4x4 mm 20-Lead QFN

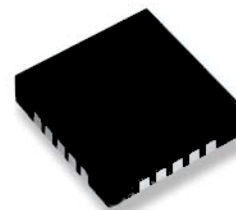


Table 1. Electrical Specifications @ +25°C, V_{DD} = 3.0 V

| Parameter | Test Conditions | Frequency | Minimum | Typical | Maximum | Units |
|-------------------------------|---|-------------------------------|---------|---------|--|----------|
| Operation Frequency | | | DC | | 4000 | MHz |
| Insertion Loss ² | | DC - 2.2 GHz | - | 1.5 | 1.75 | dB |
| Attenuation Accuracy | Any Bit or Bit Combination | DC ≤ 1.0 GHz 1.0 < 2.2 GHz | - | - | ±(0.10 + 3% of atten setting) ±(0.15 + 5% of atten setting) | dB dB |
| 1 dB Compression ³ | | 1 MHz - 2.2 GHz | 30 | 34 | - | dBm |
| Input IP3 ^{1,2} | Two-tone inputs +18 dBm | 1 MHz - 2.2 GHz | - | 52 | - | dBm |
| Return Loss | | DC - 2.2 GHz | 15 | 20 | - | dB |
| Switching Speed | 50% control to 0.5 dB of final value | | - | - | 1 | μs |

Notes: 1. Device Linearity will begin to degrade below 1 Mhz

2. See Max input rating in Table 3 & Figures on Pages 2 to 4 for data across frequency.

3. Note Absolute Maximum in Table 3.

Typical Performance Data @ 25°C, $V_{DD} = 3.0\text{ V}$

Figure 3. Insertion Loss

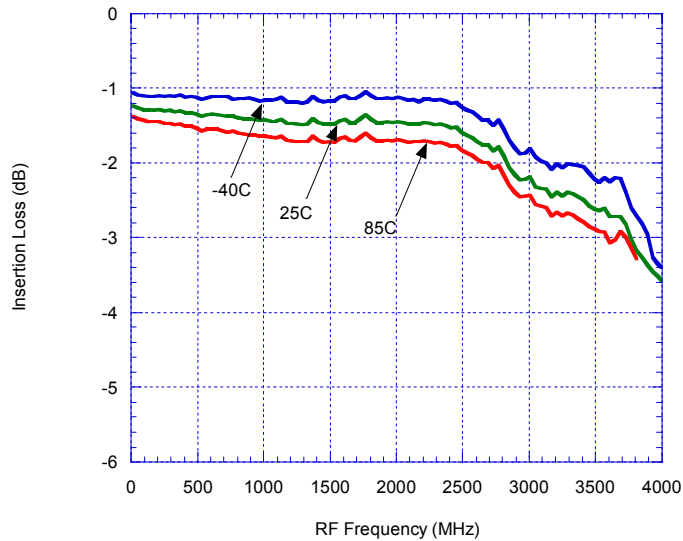


Figure 4. Attenuation at Major steps

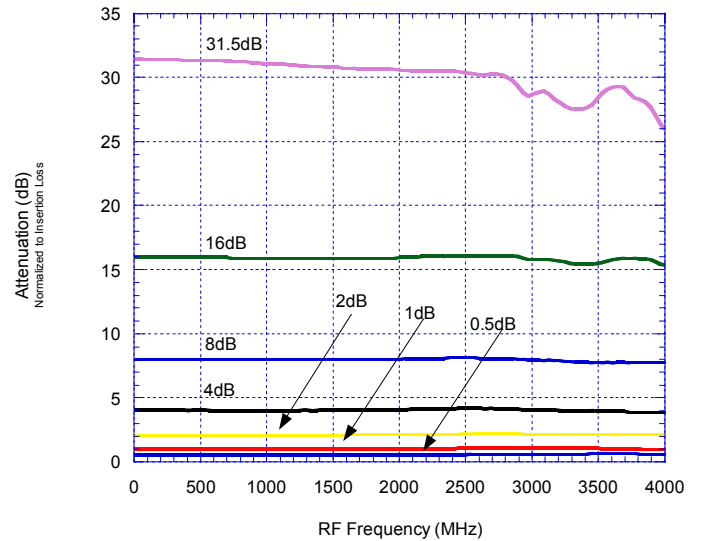


Figure 5. Input Return Loss at Major Attenuation Steps

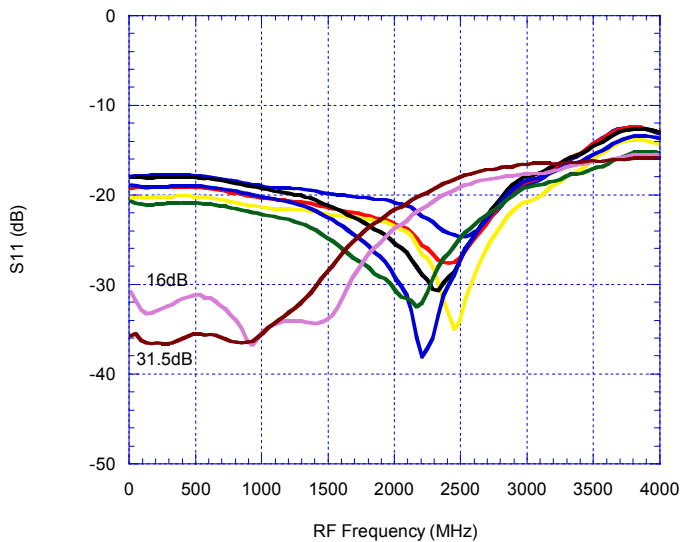
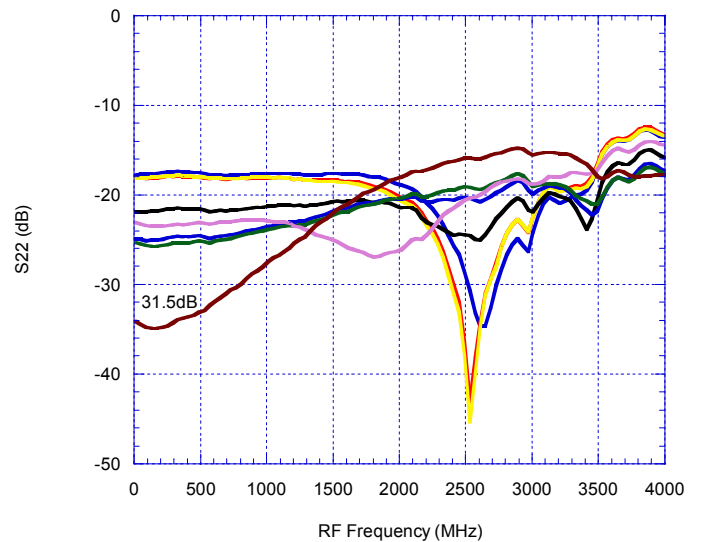


Figure 6. Output Return Loss at Major Attenuation Steps



Typical Performance Data @ 25°C, V_{DD} = 3.0 V

Figure 7. Attenuation Error Vs. Frequency

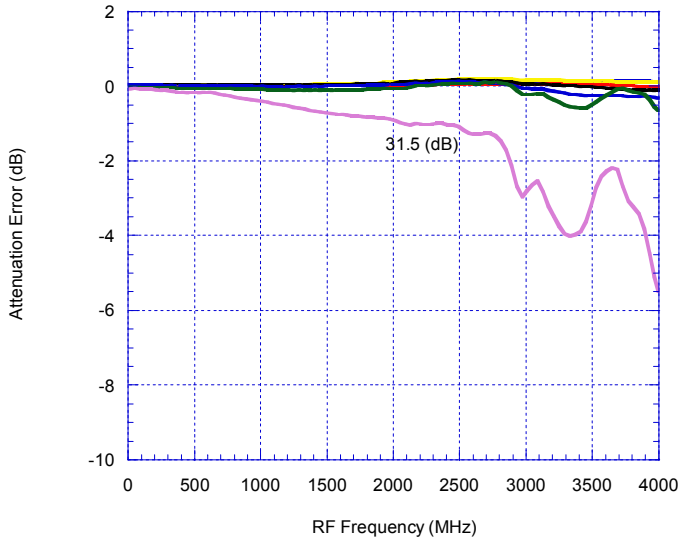


Figure 8. Attenuation Error Vs. Attenuation Setting

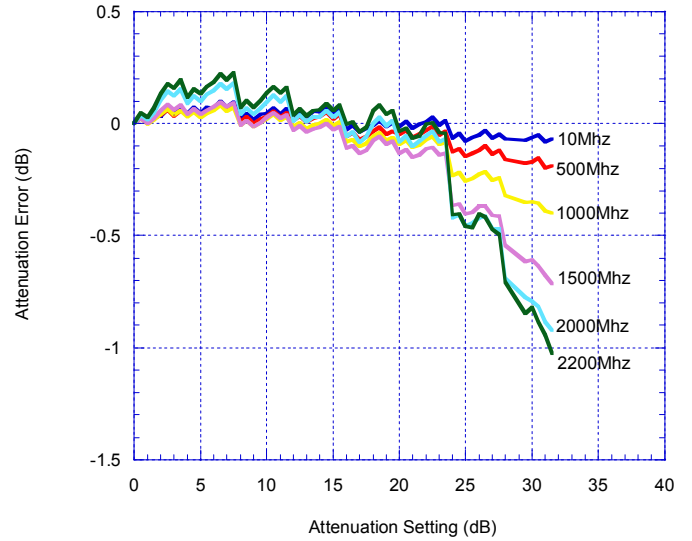


Figure 9. Attenuation Error Vs. Attenuation Setting

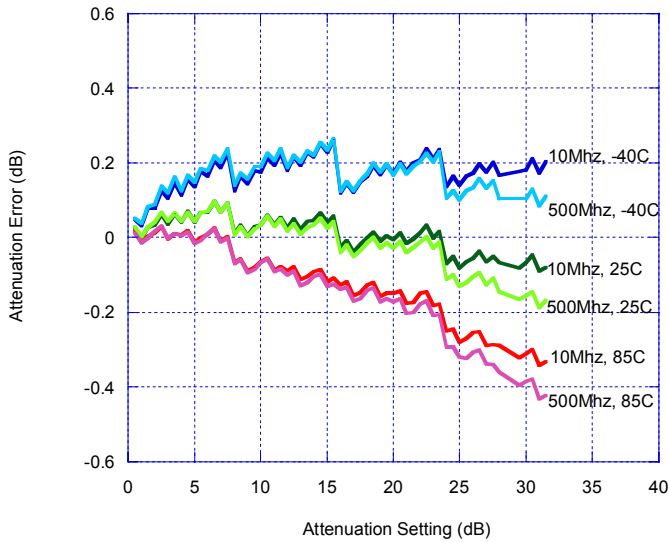
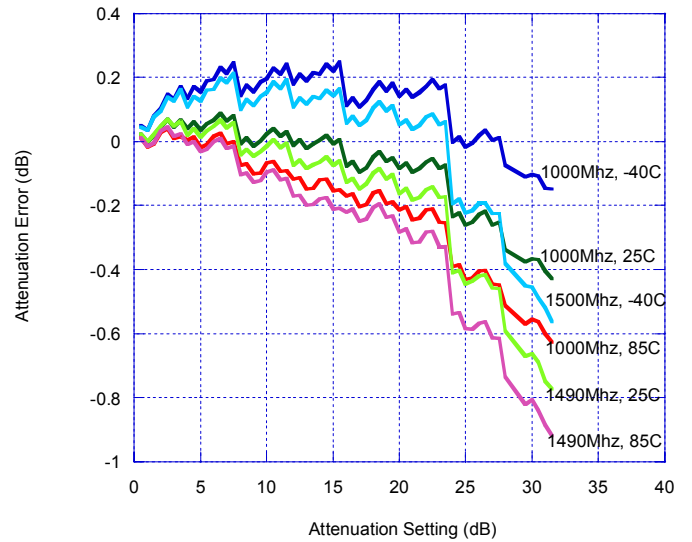


Figure 10. Attenuation Error Vs. Attenuation Setting



Note: Positive attenuation error indicates higher attenuation than target value

Typical Performance Data @ 25°C, V_{DD} = 3.0 V

Figure 11. Attenuation Error Vs. Frequency

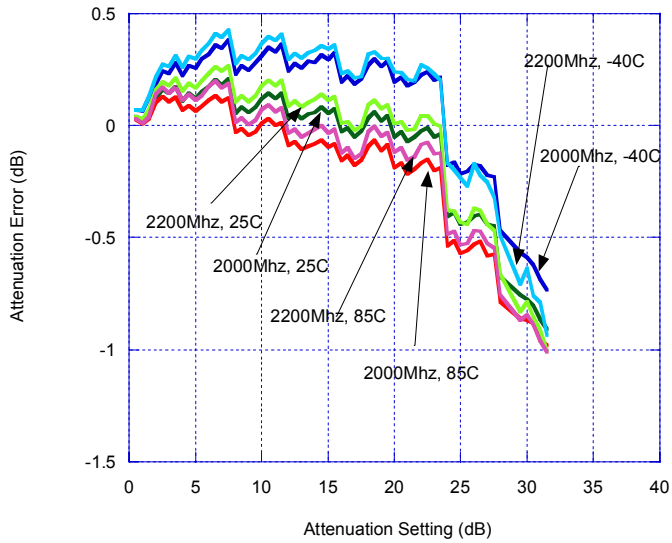


Figure 12. Input IP3 Vs. Frequency

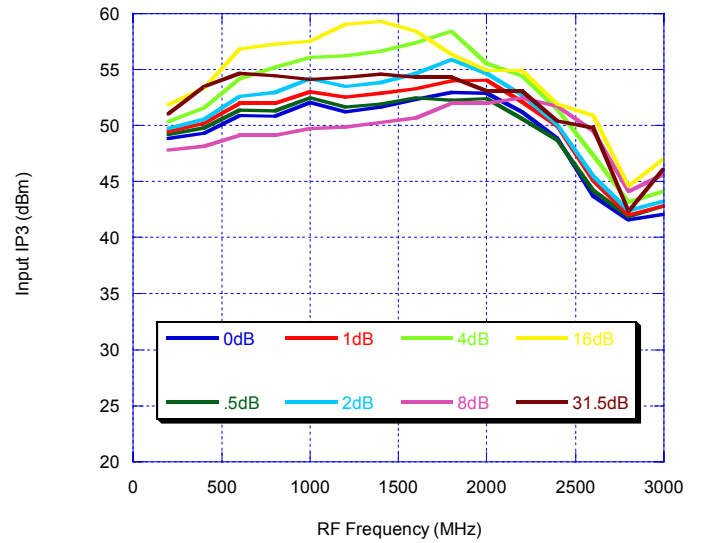
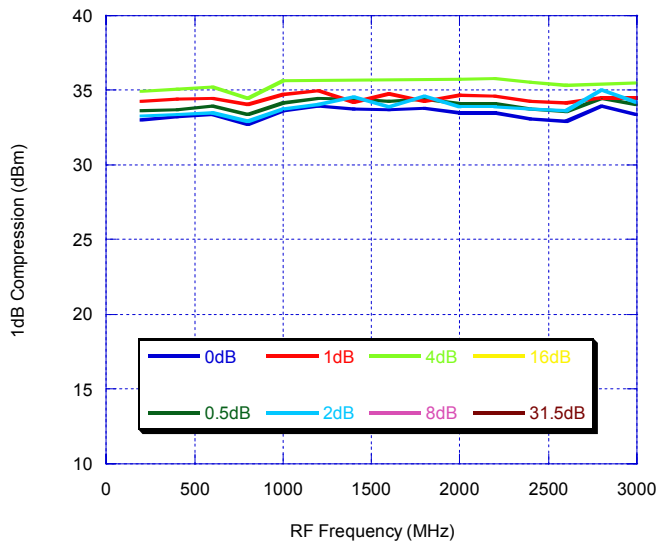


Figure 13. Input 1 dB Compression



Note: Positive attenuation error indicates higher attenuation than target value

Figure 14. Pin Configuration (Top View)

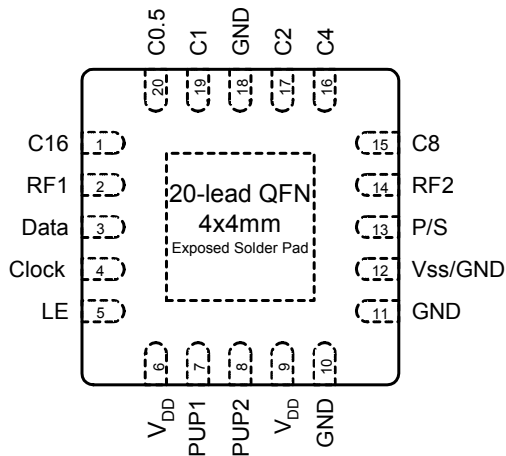


Table 2. Pin Descriptions

| Pin No. | Pin Name | Description |
|---------|----------------------|--|
| 1 | C16 | Attenuation control bit, 16dB (Note 4). |
| 2 | RF1 | RF port (Note 1). |
| 3 | Data | Serial interface data input (Note 4). |
| 4 | Clock | Serial interface clock input. |
| 5 | LE | Latch Enable input (Note 2). |
| 6 | V _{DD} | Power supply pin. |
| 7 | PUP1 | Power-up selection bit, MSB. |
| 8 | PUP2 | Power-up selection bit, LSB. |
| 9 | V _{DD} | Power supply pin. |
| 10 | GND | Ground connection. |
| 11 | GND | Ground connection. |
| 12 | V _{SS} /GND | Negative supply voltage or GND connection (Note 3) |
| 13 | P/S | Parallel/Serial mode select. |
| 14 | RF2 | RF port (Note 1). |
| 15 | C8 | Attenuation control bit, 8 dB. |
| 16 | C4 | Attenuation control bit, 4 dB. |
| 17 | C2 | Attenuation control bit, 2 dB. |
| 18 | GND | Ground connection. |
| 19 | C1 | Attenuation control bit, 1 dB. |
| 20 | C0.5 | Attenuation control bit, 0.5 dB. |
| Paddle | GND | Ground for proper operation |

Note 1: Both RF ports must be held at 0 V_{DC} or DC blocked with an external series capacitor.

- 2: Latch Enable (LE) has an internal 100 kΩ resistor to V_{DD}.
- 3: Connect pin 12 to GND to enable internal negative voltage generator. Connect pin 12 to V_{SS} (-V_{DD}) to bypass and disable internal negative voltage generator.
- 4: Place a 10 kΩ resistor in series, as close to pin as possible to avoid frequency resonance.

Table 3. Absolute Maximum Ratings

| Symbol | Parameter/Conditions | Min | Max | Units |
|------------------|--------------------------------|------|----------------------|-------|
| V _{DD} | Power supply voltage | -0.3 | 4.0 | V |
| V _I | Voltage on any DC input | -0.3 | V _{DD} +0.3 | V |
| T _{ST} | Storage temperature range | -65 | 150 | °C |
| P _{IN} | Input power (50Ω) | | +30 | dBm |
| V _{ESD} | ESD voltage (Human Body Model) | | 500 | V |

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Table 4. Operating Ranges

| Parameter | Min | Typ | Max | Units |
|--------------------------------------|---------------------|-----|---------------------|-------|
| V _{DD} Power Supply Voltage | 2.7 | 3.0 | 3.3 | V |
| I _{DD} Power Supply Current | | | 100 | μA |
| Digital Input High | 0.7xV _{DD} | | | V |
| Digital Input Low | | | 0.3xV _{DD} | V |
| Digital Input Leakage | | | 1 | μA |
| Input Power | | | +24 | dBm |
| Temperature range | -40 | | 85 | °C |

Exposed Solder Pad Connection

The exposed solder pad on the bottom of the package must be grounded for proper device operation.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS™ device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rate specified in Table 3.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS™ devices are immune to latch-up.

Switching Frequency

The SP4302 has a maximum 25 kHz switching rate.

Resistor on Pin 1 & 3

A 10 kΩ resistor on the inputs to Pin 1 & 3 (see Figure 16) will eliminate package resonance between the RF input pin and the two digital inputs. Specified attenuation error versus frequency performance is dependent upon this condition.

Programming Options

Parallel/Serial Selection

Either a parallel or serial interface can be used to control the SP4302. The P/S bit provides this selection, with P/S=LOW selecting the parallel interface and P/S=HIGH selecting the serial interface.

Parallel Mode Interface

The parallel interface consists of five CMOS-compatible control lines that select the desired attenuation state, as shown in Table 5.

The parallel interface timing requirements are defined by Figure 18 (Parallel Interface Timing Diagram), Table 9 (Parallel Interface AC Characteristics), and switching speed (Table 1).

For *latched* parallel programming the Latch Enable (LE) should be held LOW while changing attenuation state control values, then pulse LE HIGH to LOW (per Figure 18) to latch new attenuation state into device.

For *direct* parallel programming, the Latch Enable (LE) line should be pulled HIGH. Changing attenuation state control values will change device state to new attenuation. Direct Mode is ideal for manual control of the device (using hardware, switches, or jumpers).

Table 5. Truth Table

| P/S | C16 | C8 | C4 | C2 | C1 | C0.5 | Attenuation State |
|-----|-----|----|----|----|----|------|-------------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reference Loss |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0.5 dB |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 dB |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 2 dB |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 4 dB |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 8 dB |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 16 dB |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 31.5 dB |

Note: Not all 64 possible combinations of C0.5-C16 are shown in table

Serial Interface

The serial interface is a 6-bit serial-in, parallel-out shift register buffered by a transparent latch. It is controlled by three CMOS-compatible signals: Data,

Clock, and Latch Enable (LE). The Data and Clock inputs allow data to be serially entered into the shift register, a process that is independent of the state of the LE input.

The LE input controls the latch. When LE is HIGH, the latch is transparent and the contents of the serial shift register control the attenuator. When LE is brought LOW, data in the shift register is latched.

The shift register should be loaded while LE is held LOW to prevent the attenuator value from changing as data is entered. The LE input should then be toggled HIGH and brought LOW again, latching the new data. The timing for this operation is defined by Figure 17 (Serial Interface Timing Diagram) and Table 8 (Serial Interface AC Characteristics).

Power-up Control Settings

The SP4302 always assumes a specifiable attenuation setting on power-up. This feature exists for both the Serial and Parallel modes of operation, and allows a known attenuation state to be established before an initial serial or parallel control word is provided.

When the attenuator powers up in Serial mode (P/S=1), the six control bits are set to whatever data is present on the six parallel data inputs (C0.5 to C16). This allows any one of the 64 attenuation settings to be specified as the power-up state.

When the attenuator powers up in Parallel mode (P/S=0) with LE=0, the control bits are automatically set to one of four possible values. These four values are selected by the two power-up control bits, PUP1 and PUP2, as shown in Table 6 (Power-Up Truth Table, Parallel Mode).

Table 6. Parallel PUP Truth Table

| P/S | LE | PUP2 | PUP1 | Attenuation State |
|-----|----|------|------|----------------------------|
| 0 | 0 | 0 | 0 | Reference Loss |
| 0 | 0 | 1 | 0 | 8 dB |
| 0 | 0 | 0 | 1 | 16 dB |
| 0 | 0 | 1 | 1 | 31 dB |
| 0 | 1 | X | X | Defined by C0.5-C16 |

Note: Power up with LE=1 provides normal parallel operation with C0.5-C16, and PUP1 and PUP2 are not active.

Evaluation Kit

The Digital Attenuator Evaluation Kit board was designed to ease customer evaluation of the SP4302 Digital Step Attenuator.

J9 is used in conjunction with the supplied DC cable to supply VDD, GND, and -VDD. If use of the internal negative voltage generator is desired, then connect -VDD (Black banana plug) to ground. If an external -VDD is desired, then apply -3V.

J1 should be connected to the parallel port of a PC with the supplied ribbon cable. The evaluation software is written to operate the DSA in serial mode, so Switch 7 (P/S) on the DIP switch SW1 should be ON with all other switches off. Using the software, enable or disable each attenuation setting to the desired combined attenuation. The software automatically programs the DSA each time an attenuation state is enabled or disabled.

To evaluate the Power Up options, first disconnect the parallel ribbon cable from the evaluation board. The parallel cable must be removed to prevent the PC parallel port from biasing the control pins.

During power up with P/S=1 high and LE=0 or P/S=0 low and LE=1, the default power-up signal attenuation is set to the value present on the six control bits on the six parallel data inputs (C0.5 to C16). This allows any one of the 64 attenuation settings to be specified as the power-up state.

During power up with P/S=0 high and LE=0, the control bits are automatically set to one of four possible values presented through the PUP interface. These four values are selected by the two power-up control bits, PUP1 and PUP2, as shown in the Table 6.

Resistor on Pin 1 & 3

A 10 kΩ resistor on the inputs to Pin 1 & 3 (Figure 16) will eliminate package resonance between the RF input pin and the two digital inputs. Specified attenuation error versus frequency performance is dependent upon this condition.

Figure 15. Evaluation Board Layout

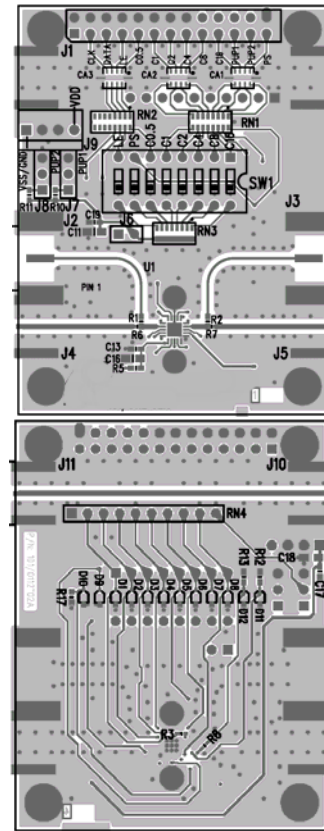
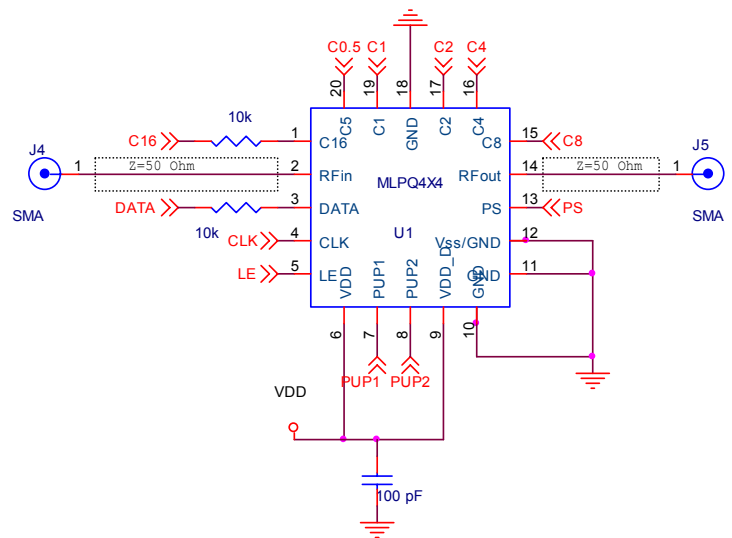


Figure 16. Evaluation Board Schematic



Note: Resistors on pins 1 and 3 are required to avoid package resonance and meet error specifications over frequency.

Figure 17. Serial Interface Timing Diagram

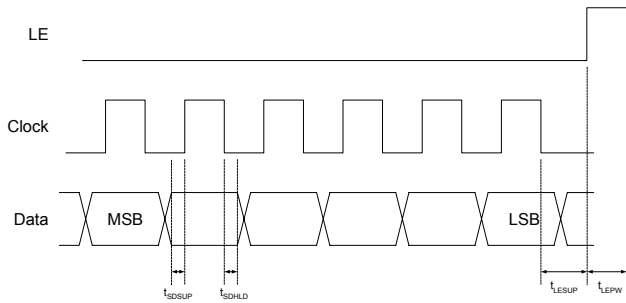


Table 7. 6-Bit Attenuator Serial Programming Register Map

| | | | | | |
|---------------------|-----------|-----------|--------------------|-----------|-----------|
| B5 | B4 | B3 | B2 | B1 | B0 |
| C16 | C8 | C4 | C2 | C1 | C0.5 |
| ↑ MSB (first in) | | | ↑ LSB (last in) | | |

Figure 18. Parallel Interface Timing Diagram

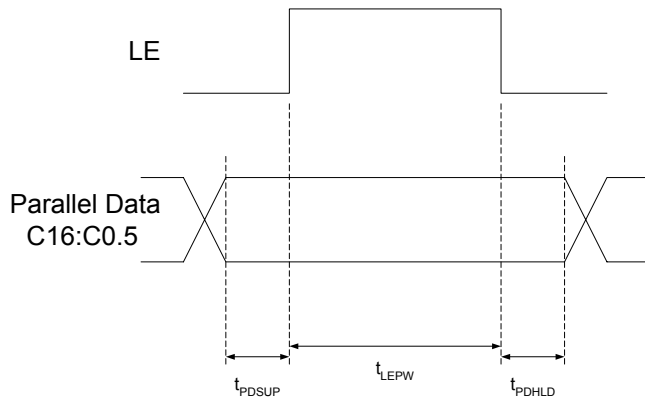


Table 8. Serial Interface AC Characteristics

$V_{DD} = 3.0\text{ V}$, $-40^\circ\text{ C} < T_A < 85^\circ\text{ C}$, unless otherwise specified

| Symbol | Parameter | Min | Max | Unit |
|-------------|--|-----|-----|------|
| f_{CLK} | Serial data clock frequency (Note 1) | | 10 | MHz |
| t_{CIKH} | Serial clock HIGH time | 30 | | ns |
| t_{CIKL} | Serial clock LOW time | 30 | | ns |
| t_{LESUP} | LE set-up time after last clock falling edge | 10 | | ns |
| t_{LEPW} | LE minimum pulse width | 30 | | ns |
| t_{SDSUP} | Serial data set-up time before clock rising edge | 10 | | ns |
| t_{SDHLD} | Serial data hold time after clock falling edge | 10 | | ns |

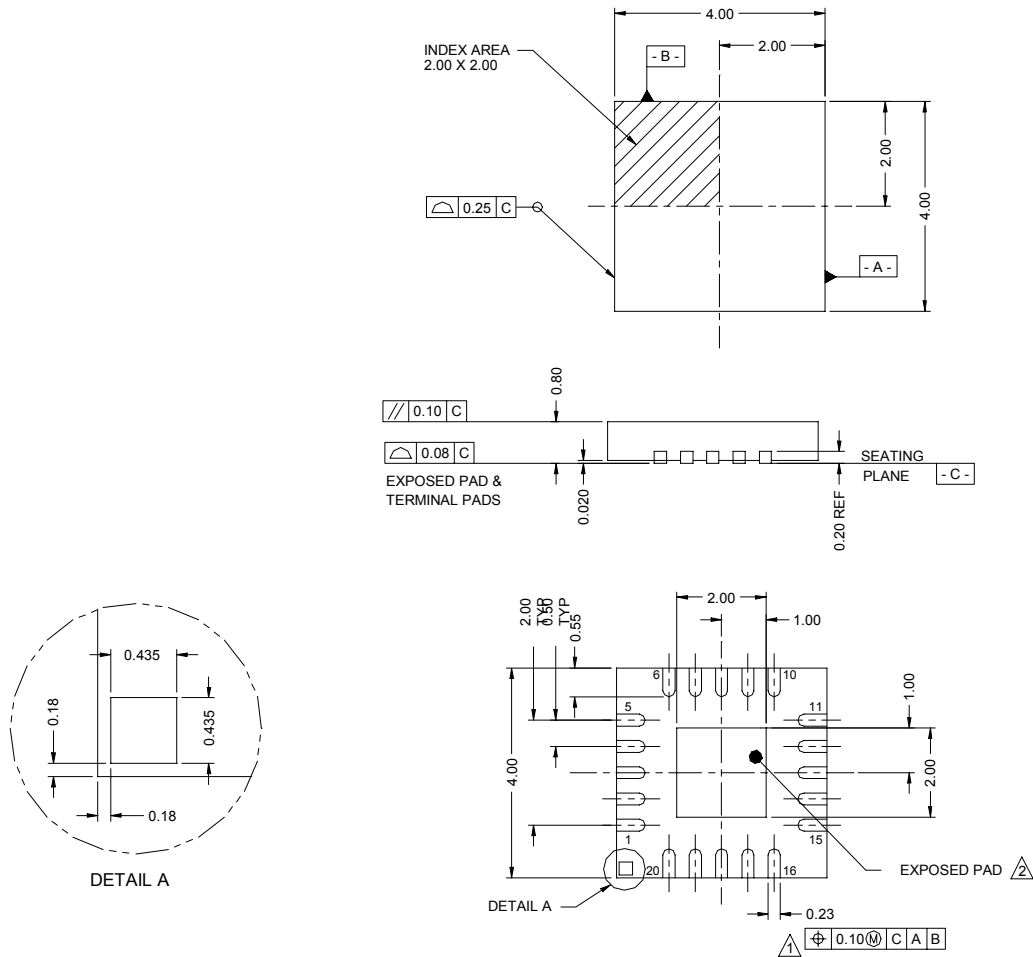
Note: f_{CLK} is verified during the functional pattern test. Serial programming sections of the functional pattern are clocked at 10 MHz to verify fclk specification.

Table 9. Parallel Interface AC Characteristics

$V_{DD} = 3.0\text{ V}$, $-40^\circ\text{ C} < T_A < 85^\circ\text{ C}$, unless otherwise specified

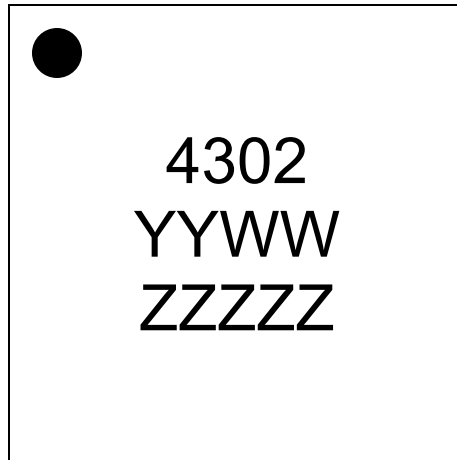
| Symbol | Parameter | Min | Max | Unit |
|-------------|---|-----|-----|------|
| t_{LEPW} | LE minimum pulse width | 10 | | ns |
| t_{PDSUP} | Data set-up time before rising edge of LE | 10 | | ns |
| t_{PDHLD} | Data hold time after falling edge of LE | 10 | | ns |

Figure 19. Package Drawing



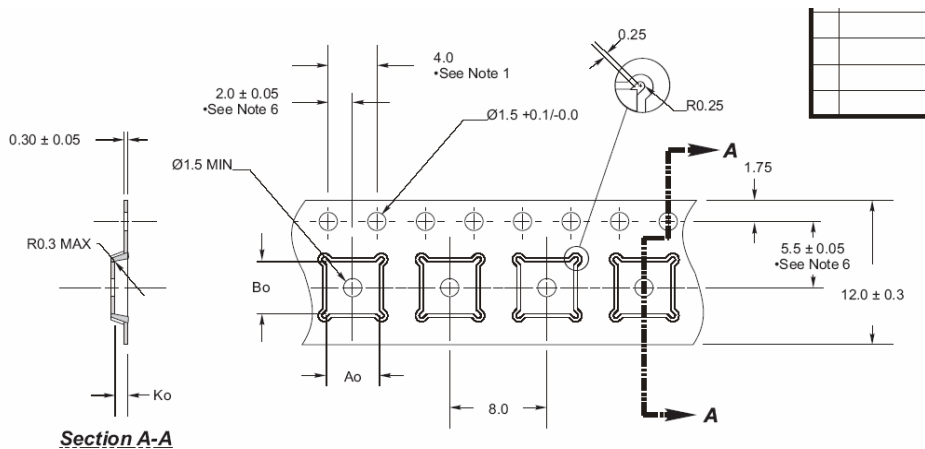
1. Dimension applies to metallized terminal and is measured between 0.25 and 0.30 from terminal tip.
2. Coplanarity applies to the exposed heat sink slug as well as the terminals.
3. Dimensions are in millimeters.

Figure 20. Marking Specifications



YYWW = Date Code
ZZZZZ = Last five digits of PSC Lot Number

Figure 21. Tape and Reel Drawing



Ao = 4.35 mm
Bo = 4.35 mm
Ko = 1.1 mm

- Notes:
1. 10 sprocket hole pitch cumulative tolerance ± 0.2 .
 2. Camber not to exceed 1mm in 100mm.
 3. Material: PS + C.
 4. Ao and Bo measured as indicated.
 5. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
 6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.